

1	VL1	Characterization analysis of a High Speed, Low Resolution ADC based on Simulation results for different resolutions	Baljit Singh Parveen Klair	MIET, Jammu, J & K(India) BCET, Gurdaspur, Punjab(India)
2	VL2	Spurious Power Suppression Technique (SPST) based High-Speed Low-Power Functional Unit	R.Madhumathi A.Latha P.Meenakshi Vidya	Easwari Engineering College Bharathi Salai, Ramapuram,Chennai, India
3	VL3	Verification of RAM at SoC	Sandip Patel S. K. Hadia	V. T. Patel Department of E.C.E Charotar Institute of Technology Changa, Gujarat, INDIA – 388 421
4	VL21	IMPLEMENTATION OF FUZZY LOGIC BASED AUTOMATIC CANE CRUSHING MILL CONTROLLER IN FPGA	Yogesh Misra ¹ Dr. Pratibha Misra ²	1Faculty of Engineering & Technology Mody Institute of Technology & Science (Deemed University), Rajasthan, India. 2National Sugar Institute, Kanpur, India
5	VL29	POWER REDUCTION TECHNIQUE FOR CONTENT ADDRESSABLE MEMORY CIRCUITS	V.Sumalatha P.Ankith Kumar	JNTU-Anantapur
6	VL31	VHDL Implementation of JPEG2000 Encoder	Kanchan H. Wagh	St. Vincent Pallotti College of Engg. and Technology , Gavsi Manapur , Nagpur
7	VL32	FPGA Based Design of Direct Digital Synthesizer	Dr. R. K. Sharma ¹ Gargi Upadhyaya ² Amit Agarwal ³	^{1,2} NIT Kurukshetra ³ Wipro Technologies
8	VL33	Power Reduction Technique for LFSR Reseeding Scheme	K.Kishore E.V.Narayana	
9	VL38	Inexact Hamming Weight Threshold Voters for FPGA based System Design	Bharghava Abinesh Suresh Purini Govindarajulu	Center for VLSI & Embedded System Technologies, International Institute of Information Technology, Hyderabad
10	VL43	Design of a Pedometer using Programmable System On Chip	Nandakumar.R K.S.Lalmohan Sreejeesh.S.G	DOEACC Centre Calicut, INDIA
11	VL47	Realizability of Linear Temporal Logic Specifications: An Experimental Study	Moumita Das Ansuman Banerjee Subhashis Majumder	IERCEM IIT, Kolkata Interra Systems India Heritage Institute of Technology, Kolkata

12	VL55	SIGNAL INTEGRITY ENGINEERING REDEFINED TO INCLUDE RF STAGES DEPLOYING CMOS VLSI DEVICES (AS IN BLUETOOTH™)	P. S. Neelakanta, Ph. D., C. Eng., Fellow IEE Bethany J. Talbot, M. S. E.E Diana Portal M. S. E. E.	Florida Atlantic University, Boca Raton, Florida 33431, USA
13	IP3	2D to 3D Conversion	Mr. Akash I. Mecwan Mr. Dipesh Panchal Mr. Dhaval Shah	Nirma University, Ahmedabad.Gujarat
14	CO6	PERFORMANCE ANALYSIS OF BROADBAND OFCDM SYSTEM FOR WIRELESS COMMUNICATIONS	Mr. Siva Sundhara Raja Ms.Vigneshwarar MR.D.Siva	SACS Engg.College, Madurai. RAJA Engg.College, Madurai.
15	CO7	CAC Framework with QoS support for IEEE 802.16 (WIMAX) Broadband Wireless Network	Mr. Veeranna D Ms. Jigisha N Patel	SVNIT Surat-395007[INDIA]
16	CO13	Evaluation of Wireless Sensor Networks Routing Protocols	Gaurang Raval ¹ Maniel Shah ² Keyur Panchal ³	1Institute of Technology Nirma University,Ahmedabad. ² Infrastructure Management Services Infosys Technologies Ltd.Pune. ³ Transformation Solutions Group Infosys Technologies Ltd.Pune
17	CO18	Hybrid Optical Wireless Networks	D. Sheela C.Chellamuthu	Tagore Engineering College, Anna University, Chennai, India R.M.K. Engineering College, Anna University, Chennai, India
18	CO19	Performance Analysis of WLAN's MAC Access Mechanism	Lakshmanan. M Noor Mohammed.V Rajesh. R Nandakumar. S	School of Electrical Sciences, VIT University, Vellore, India
19	CO25	JPEG IMAGE COMPRESSION & TRANSMISSION OVER WIRELESS CHANNEL	Vaibhavi P.Lineswala Ms. Jigisha N. Patel	SVNIT, Icchanath, Surat, India
20	CO31	Average Error Rate of a Two-Hop Amplify-and-Forward Relay Scheme in Composite Fading Channels	Valentine A. Aalo,Ph.D. ¹ George.P.Efthymoglou,Ph.D ²	¹ Florida Atlantic University, Boca Raton, Florida 33431, USA ² 80 Karaoli & Dimitriou Street, Piraeus 18534, Greece